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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,160	03/10/2004	Chih-Feng Sung	250122-1380	8124

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EXAMINER	
DHARIA, PRABODH M	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,160	SUNG, CHIH-FENG	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,4,7,8,11,12,15 and 16* is/are allowed.

6)☒ Claim(s) *1,2,5,6,9,10,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01-03-07,10-18-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 03-10-2004 and 10-18-2004 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1,2,5,6,9,10,13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Libsch et al. (US 2003/0107565 A1) in view of Nathan et al. (US 2006/0027807A1).

Regarding Claims 1, 2, 5, 6, 9, 10, 13 and 14 Libsch et al. teaches a pixel structure of an active matrix organic light-emitting diode (OLED) display (page 1, paragraph 09, Lines 1-4), comprising: a first transistor having a gate terminal coupled to a scan signal (see figure 5a, page 5, paragraph 76) and a drain terminal coupled to a data signal (see figure 5a, page 5, paragraph

74); a storage capacitor having two terminals coupled to a source terminal of the first transistor (page 2, paragraph 36, Lines5, 6 see figure 3, item # CS1)

However, Libsch et al. fails to recite or disclose a reference node respectively, the reference node having a second voltage; a second transistor having a gate terminal coupled to the source terminal of the first transistor and a source terminal coupled to the reference node; and an OLED having a cathode coupled to a drain terminal of the second transistor and an anode coupled to a first voltage exceeding the second voltage; wherein the second transistor is an amorphous silicon thin film transistor (a-Si TFT), and an equivalent channel width/length (W/L) ratio of the second transistor exceeds 10.

However, Natahan et al. teaches a storage capacitor having two terminals coupled to a source terminal of the first transistor and a reference node respectively (see figure 5A, page 3, paragraph 35) the reference node having a second voltage (see figure 5A, page 3, paragraph 35); a second transistor having a gate terminal coupled to the source terminal of the first transistor (see figure 5A, page 3, paragraph 35); and a source terminal coupled to the reference node (see figure 5A, page 3, paragraph 35); and an OLED having a cathode coupled to a drain terminal of the second transistor and an anode coupled to a first voltage exceeding the second voltage (see figure 5A, page 3, paragraph 35 V_{DD} > GND); wherein the second transistor is an amorphous silicon thin film transistor (a-Si TFT) (page 1, paragraph 11, Lines 1,2), and an equivalent channel width/length (W/L) ratio of the second transistor exceeds 10 (page 3, paragraph 38, teaches the W/L can be scaled to any value as the overall structure achieves high density pixel integration and page 2, paragraph 30 right side column Lines 9-15, teaches cost savings, page 3, paragraph 36, Lines 13-17 current required to drive OLED where width of the second transistor

has to be large enough to light OLED display) and Natahan et al. teaches the second voltage is a ground or a low voltage (see figure 5A, 6A, 12-16, page 3, paragraph 35).

The reason to combine is the active matrix display are well known in the art and Libsch et al. teaches the active matrix OLED display, however Libsch et al. fails to recite specific pixel structure which is specifically elaborated by Nathan et al. with amorphous silicon transistors.

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Nathan et al. in the teaching of Libsch et al. to be able to have an OLED display with amorphous silicon transistors driver circuit IC with significant saving in capital equipment and lowers overall cost of the display (page 2, paragraph 30 right hand side column Lines 9-13).

Allowable Subject Matter

5. Claims 3,4,7,8,11,12,15 and 16 are allowed.

6. The following is an examiner's statement of reasons for allowance:

a plurality of driving transistors connected in parallel, each having a gate terminal coupled to the source terminal of the switching transistor, a source terminal coupled to the reference node, and a drain terminal; and an OLED having a cathode coupled to the drain terminals of the driving transistor and an anode coupled to a first voltage exceeding the second voltage; wherein the driving transistors are amorphous silicon thin film transistors (a-Si TFT), wherein the relationship between an equivalent channel width/length (W/L) ratio R of the driving transistor and the number of driving 10 transistors N is R>10/N.

The prior arts cited of Nathan et al. and all the other cited prior arts on 892's fail to recite or disclose the uniquely distinct features represented by underlined bold claimed limitations above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kung et al. (US 2003/0234392 A1) Active matrix organic light emitting diode dispaly pixel structure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

9. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

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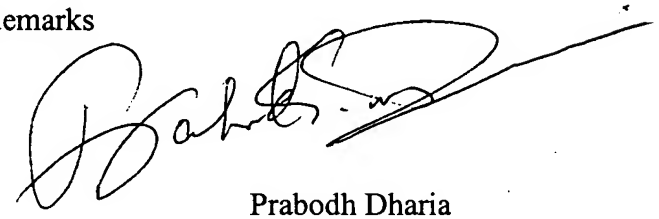
Washington, D.C. 20231



Prabodh Dharia

Partial Program Signatory Authority

AU2629

January 03, 2007